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Document Listing

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Document Listing

Document	Selected Pages	Page Range
US20020068427	12	1 - 12
US006207222	15	1 - 15
US006120844	12	1 - 12
US006106678	13	1 - 13
US006066358	13	1 - 13
Total (5)	65	-

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Document Listing

Document	Selected Pages	Page Range
US005366929	11	1 - 11
Total (1)	11	-

L Number	Hits	Search Text	DB	Time stamp
1	37	dielectric and (bottom adj up) with (growth or deposition)	USPAT; US-PGPUB	2002/07/17 15:10
2	2504	(silicon adj oxide) same plasma with deposition	USPAT; US-PGPUB	2002/07/17 15:10
3	155	((silicon adj oxide) same plasma with deposition) and TEOS and "O.sub.3"	USPAT; US-PGPUB	2002/07/17 15:11
4	58	(((silicon adj oxide) same plasma with deposition) and TEOS and "O.sub.3") and ((via or trench or opening or hole or recess) with (silicon adj oxide))	USPAT; US-PGPUB	2002/07/17 15:12
5	32	(((silicon adj oxide) same plasma with deposition) and TEOS and "O.sub.3") and ((via or trench or opening or hole or recess) with (silicon adj oxide)) and @ad<=20001031	USPAT; US-PGPUB	2002/07/17 15:14

US-PAT-NO: 6413583

DOCUMENT-IDENTIFIER: US 6413583 B1

TITLE: Formation of a liquid-like silica layer by reaction of an organosilicon compound and a hydroxyl forming compound

---------- PRIOR ART ----------

U.S. Pat. No. 5,536,741, issued Jan. 14, 1997, describes a gap fill process using **silicon oxide** layers produced by combining organosilicon compounds such as tetraethoxysilane (**TEOS**, also known as tetraethylorthosilicate) with oxygen and/or ozone. The process can include an optional source of water, such as water vapor, hydrogen peroxide, or an alcohol that forms water when oxygenated. The gap fill layers are deposited subsequent to **plasma** enhanced **deposition** of a conformal layer from the same components by turning off a power source used to form a **plasma**. The presence of water in the reactor was believed to result in a slightly improved gap fill process.

U.S. Pat. No. 5,610,105, issued Mar. 11, 1997, describes an intermetal dielectric layer produced by low temperature PECVD of **TEOS** and water, followed by annealing in an oxygen atmosphere to densify the dielectric layer.

U.S. Pat. No. 5,710,079, issued Jan. 20, 1998, describes a gap fill process using silicon oxide layers produced by combining organosilicon compounds such as **TEOS** with ozone and water using UV light to decompose the ozone. Rapid decomposition of the ozone was assumed to form atomic oxygen that combines with

water to form peroxide.

U.S. Pat. No. 5,360,646, issued Nov. 1, 1994, describes a gap fill process using silicon oxide layers produced by combining **TEOS** with acetic acid. The highly electronegative oxygen in **TEOS** reacts with hydrogen from the acetic acid to form hydroxyl groups within the deposited silicon oxide film.

The present invention provides a method and apparatus for uniformly depositing a **silicon oxide** layer having a low dielectric constant for use as a gap fill layer, a pre-metal dielectric layer, an inter-metal dielectric layer, or a shallow **trench** isolation dielectric layer in sub-micron devices. The method comprises reacting one or more silicon compounds that contain carbon (i.e., organosilicon compounds) with a hydroxyl forming compound at a substrate temperature less than about 400.degree. C. The organosilicon compounds preferably contain one or more silicon-carbon bonds that remain in the deposited dielectric layers after reaction with a hydroxyl forming compound such as hydrogen peroxide or dimethyldioxirane. The hydroxyl forming compound may be produced prior to, or during deposition, such as by oxidation of water using ozone and UV light, by reaction of acetone and potassium monoperoxy sulfate to form dimethyldioxirane, or by oxidation of an organic compound that forms hydroxyls, such as oxidation of isopropyl alcohol with ozone or oxygen to produce acetone and hydrogen peroxide. In addition, the hydroxyl forming compound could be an acid such as acetic acid that provides hydrogen that reacts with siloxane compounds to form hydroxyl groups, or an acid compound that reacts with water to form hydroxyl compounds.

The organosilicon compounds that produce uniform, low k dielectric layers
preferably include one or more silicon-hydrogen bonds such as methylsilane,
CH.sub.3 SiH.sub.3, dimethylsilane, (CH.sub.3).sub.2 SiH.sub.2,
trimethylsilane, (CH.sub.3).sub.3 SiH, and
1,1,3,3-tetramethyldisiloxane,
(CH.sub.3).sub.2 --SiH--O--SiH--(CH.sub.3).sub.2. Gap fill layers can also be
uniformily deposited from other organosilicon compounds such as
tetramethylsilane, (CH.sub.3).sub.4 Si, and
tetraethylorthosilicate (**TEOS**).
The silicon oxide layers are cured at low pressure and high temperature to
stabilize film properties such as moisture content.

The present invention provides a method and apparatus for uniformly depositing
a silicon oxide layer having a low dielectric constant (<<lt;about 4). The
silicon oxide layer is produced by reacting an organosilicon compound, such as
an organosilane or organosiloxane, with a hydroxyl forming compound such as
H.sub.2 O.sub.2, dimethyldioxirane, acetic acid, or water at a substrate
temperature less than about 400.degree. C. The **silicon oxide** layer can be used
as a gap fill layer, a pre-metal dielectric layer, an inter-metal dielectric
layer, and a shallow **trench** isolation dielectric layer in sub-micron devices.
The silicon oxide layer is cured at temperatures less than about 500.degree.
C. to form a carbon doped silicon oxide film.

When a gap fill layer is deposited on a liner layer, the liner layers are
preferably prepared by oxidizing an organo silicon compound, such as listed
above, with oxygen (O.sub.2) or oxygen containing compounds such as nitrous
oxide (N.sub.2 O), ozone (**O.sub.3**), or carbon dioxide (CO.sub.2), preferably
O.sub.2 or N.sub.2 O, such that the carbon content of the

deposited film is
from about 1 to about 50% by atomic weight, preferably from about 5 to about
30%. The oxidized organo silicon layer has a dielectric constant of about 3.0
and has excellent barrier properties. The oxidized organo silicon layers
further have high oxide content in comparison to conventional low k dielectric
layers and good adhesion properties.

Oxidizing compounds are preferably dissociated to increase reactivity prior to
entering a reaction chamber. RF power can also be coupled to the deposition
chamber to increase dissociation of the oxidizing compounds. The oxidizing
compounds may also be dissociated in a remote microwave chamber or remote
plasma chamber prior to entering the **deposition** chamber to reduce excessive
dissociation of the silicon containing compounds. Deposition of the **silicon
oxide** layer can be continuous or discontinuous. Although deposition preferably
occurs in a single deposition chamber, the layer can be deposited sequentially
in two or more deposition chambers. Furthermore, RF power can be cycled or
pulsed to reduce heating of the substrate and promote greater porosity in the
deposited film. During deposition of the **silicon oxide** layer, the substrate is
maintained at a temperature of from about -20.degree. C. to about 400.degree.
C., and preferably is maintained at a temperature of approximately -20.degree.
C. to 40.degree. C.

For the gap fill layers, an organosilicon compound as described above is
oxidized during deposition by reaction with a hydroxyl forming compound such as
by reaction with hydrogen peroxide (H.sub.2 O.sub.2), which can be produced in
the reaction system by combining ozone (**O.sub.3**) and water (H.sub.2 O).sub.2

preferably in the presence of UV light having a wavelength of about 254
nanometers as described in U.S. Pat. No. 5,710,079 (which is incorporated by
reference herein), by reaction with an oxirane compound such as
dimethyldioxirane as described below, by oxidation of an organic compound as
described in U.S. Pat. No. 4,303,632 (which is incorporated by reference
herein), or by reaction with acetic acid as described in U.S. Pat. No.
5,360,646 (which is incorporated by reference herein). The hydroxyl forming
compounds are also preferably dissociated in a remote RF or microwave chamber.
Preferably, the gap fill layer has a carbon content that is from about 1 to
about 50 by atomic weight, most preferably about 5 to about 30%. During
deposition of the gap fill layer, the substrate is maintained at a temperature
from about -20.degree. C. to about 400.degree. C., and preferably a
temperature from about -20.degree. C. to about 40.degree. C. for
organosilicon compounds containing Si--C bonds. After curing at a temperature
greater than about 400.degree. C., the gap fill layer has a dielectric
constant less than-about 3.5. The oxidized organo silicon layers further have
good adhesion properties.

One suitable CVD reactor in which a method of the present invention can be
carried out is shown in FIG. 2, which is a vertical, cross-section view of a
parallel plate chemical vapor deposition reactor 10 having a high vacuum region
15. Reactor 10 contains a gas distribution manifold 11 for dispersing process
gases through perforated holes in the manifold to a substrate or wafer (not
shown) that rests on a substrate support plate or susceptor 12 which is raised
or lowered by a lift motor 14. A liquid injection system

(not shown), such as typically used for liquid injection of **TEOS**, may also be provided for injecting a liquid organosilane and/or organosiloxane compound. The preferred organosilicon compounds are gases.

The oxidized organosilane or organosiloxane layer of the present invention can be used to replace **silicon oxide** layers in most applications. An embodiment that demonstrates the versatility of the present invention is a three-layer gap fill process as shown in FIG. 6 using the reactor of FIG. 1. Referring to FIG. 6, a substrate is positioned 200 in the reactor 10 and an oxidized organosilane layer having a low dielectric constant is deposited 205 by a PECVD process from a **plasma** comprising an organosilane compound and/or an organosiloxane compound, and an oxidizing gas such as O.sub.2 or N.sub.2 O. The **deposition** step 205 can include a capacitively coupled **plasma** or both an inductively and a capacitively coupled **plasma** in the chamber 15 according to methods known in the art. An inert gas such as helium is commonly used in the PECVD process to assist in plasma generation. A gap fill layer is then deposited 210 on the liner layer in accordance with the present invention, preferably by reacting an organosilane or organosiloxane compound used to produce the liner layer with a hydroxyl forming compound. The gap fill layer is preferably self-planarizing, and preferably is hydrophobic after curing to remove water. A cap layer is then deposited 215 on the gap fill layer, preferably using the same process for depositing the liner layer. The substrate is then removed 220 from the reactor 10.

Trimethylsilane, (CH.sub.3).sub.3 SiH, at 500 sccm
Isopropyl Alcohol, at 1000

mg/min Ozone, O.sub.2 with 12 wt % **O.sub.3**, at 3000 sccm
Helium, He, at 4000
sccm

reacting a silicon compound selected from a group
consisting of methylsilane,
dimethylsilane, trimethylsilane, and combinations thereof,
with a hydroxyl
forming compound produced from an oxidizing gas comprising
oxygen (O.sub.2) and
about 6-20 wt % of ozone (**O.sub.3**) to deposit a film
comprising silicon-carbon
bonds on a patterned semiconductor substrate; and

depositing a first dielectric layer comprising silicon,
oxygen, and carbon from
process gases comprising trimethylsilane and a hydroxyl
forming compound
produced from an oxidizing gas comprising oxygen (O.sub.2)
and about 6-20 wt %
of ozone (**O.sub.3**);

L Number	Hits	Search Text	DB	Time stamp
1	13	dielectric same ((bottom adj up) with (growth or deposition))	USPAT; US-PGPUB	[illegible]
2	0	dielectric same ((bottom adj up) with (growth or deposition))	EPO; JPO; DERWENT; IBM_TDB	[illegible]
3	1	dielectric and ((bottom adj up) with (growth or deposition))	EPO; JPO; DERWENT; IBM_TDB	[illegible]
4	37	dielectric and ((bottom adj up) with (growth or deposition))	USPAT; US-PGPUB	2002/07/17 10:39
5	24	(dielectric and ((bottom adj up) with (growth or deposition))) not (dielectric same ((bottom adj up) with (growth or deposition)))	USPAT; US-PGPUB	2002/07/17 10:39

US-PAT-NO: 6106678

DOCUMENT-IDENTIFIER: US 6106678 A

TITLE: Method of high density plasma CVD gap-filling

---------- KWIC ---------

Plasma enhanced chemical vapor deposition (PECVD) has been used for depositing intermetal **dielectric** layers at low temperatures in integrated circuit applications. A publication by M. Gross et al entitled "Silicon dioxide trench filling process in a radio-frequency hollow cathode reactor", J. Vac. Sci. Technol. B 11(2), March/April 1993, describes a process for void-free silicon dioxide filling of trenches using a hollow cathode reactor wherein silane gas is fed through a top target which supports a low frequency (1 MHz), low pressure (.about.0.2 Pa) oxygen and xenon discharge. In this process, high ion bombardment and a low rate of gas phase reaction produce an ion induced reaction with surface adsorbates, leading to directional oxide film growth whereby trenches with one micron openings and aspect ratios up to 2.5:1 are filled at rates over 400 A/min.

A publication by P. Shufflebotham et al. entitled "Biased Electron Cyclotron Resonance Chemical-Vapor Deposition of Silicon Dioxide Inter-Metal **Dielectric** Thin Films," Materials Science Forum Vol. 140-142 (1993) describes a low-temperature single step gap-filled process for use in inter-metal **dielectric** (IMD) applications on wafers up to 200 mm in diameter wherein sub-0.5 micron high aspect ratio gaps are filled with

SiO.sub.2 utilizing an
O.sub.2 --Ar--SiH.sub.4 gas mixture in a biased electron cyclotron resonance
plasma-enhanced chemical-vapor deposition (ECR-CVD) system. That single step
process replaced sequential gap-filling and planarization steps wherein TVD
SiO.sub.2 was subjected to plasma etch-back steps, such technique being
unsuitable for gap widths below 0.5 microns and aspect ratios (gap
height:width) above 1.5:1.

Microwave energy represented by arrow 14 travels through **dielectric** window 15
and enters the plasma generating chamber 3, the walls of which are water cooled
by water supply conduit 17. Electromagnetic coils 18 below substrate holder 7
are used for shaping the magnetic field in the vicinity of the substrate 6. A
DC power source 19 provides power to the substrate holder 7 for
electrostatically clamping substrate 6.

In order to provide a vacuum in chamber 21, a turbo pump is connected to outlet
port 30 and a pressure control valve can be used to maintain the desired vacuum
pressure. Reactants such as an oxygen-containing reactant (e.g., oxygen) and a
silicon-containing reactant (e.g., silane) can be supplied into the chamber by
conduits 31, 32 which feed the reactant gases to a gas distribution ring
extending around the underside of **dielectric** window 33 or the reactants can be
supplied through a **dielectric** showerhead window. A TCP coil 34 located outside
the chamber in the vicinity of the window is supplied RF power by RF source 35
and associated circuitry 36 for impedance matching, etc. When a substrate is
processed in the chamber, the RF source 35 supplies the TCP coil 34 with RF
current at 13.56 MHz and the RF source 26 supplies the lower electrode with RF

current at 410 kHz.

Film stoichiometry determines many important film properties such as stress, OH content, refractive index, **dielectric** constant, breakdown voltage, density, etc. The film stoichiometry depends on the relative concentrations of oxygen ions and the adsorbed SiH.sub.x species responsible for film growth. In practice, the O.sub.2 to SiH.sub.4 gas flow ratio is the most direct external control of this ratio. For instance, as the O.sub.2 /SiH.sub.4 ratio increases, OH content increases and refractive index decreases. The optimum reaction for stoichiometric SiO.sub.2 is represented by the reaction O.sub.2 +SiH.sub.4 .fwdarw.SiO.sub.2 +2H.sub.2, which results in minimal Si--OH and Si--H incorporation in the film. Lowering the O.sub.2 /SiH.sub.4 ratio below unity starves the reaction of oxygen, and excess silicon begins to appear in the oxide. Wafer temperature can also affect properties normally controlled through the film stoichiometry. For instance, reduced stress can be obtained at lower wafer temperatures.

uniformity of .ltoreq.1.6%, deposition rate of 5300 .ANG./min, breakdown strength of .gtoreq.8 MV/cm, **dielectric** constant of 4.1+-0.1, stress (compressive) of 100.+-.50 MPa, refractive index at 6328 .ANG. of 1.485.+-.0.015, OH content of .ltoreq.0.5 atomic %, H.sub.2 O content of below its detection limit and particulate density of .ltoreq.0.3 cm.sup.-3.

The gap-fill process according to the invention can also be carried out with the apparatus shown in FIG. 2 as follows. The reaction chamber can comprise a short cylindrical vacuum chamber evacuated with a side mounted turbo molecular

pump providing a pumping speed of approximately 550 liters/second. The O.sub.2 and SiH.sub.4 reactant gases can be introduced through separate gas rings located at the outer edge of the TCP window. Plasma can be generated using a TCP source consisting of a spiral coil operated at 13.56 MHz. Such TCP sources couple RF power into the plasma inductively through a **dielectric** window, generating a planar, high density plasma at low pressures. Wafers can be mechanically clamped at their outside edge onto an aluminum electrode located 10 cm from the TCP window. The temperature of the electrode can be maintained at 10.degree. C. and wafer temperature control can be accomplished through the application of static He pressure to the backside of the wafer. A large DC sheath voltage above the surface of the wafer can be provided by supplying RF power to the electrode.

The use of TCP-CVD for depositing high-quality SiO.sub.2 inter-metal **dielectric** (IMD) in sub-half micron, high aspect ratio gaps involves simultaneous deposition and sputtering of SiO.sub.2. The resultant anisotropic **deposition** fills gaps from the **bottom-up** and the angular dependence of the sputtering yield also prevents the tops of the gaps from pinching off during **deposition**. Sputtering is produced through the application of a large RF bias to the wafer. The bias power determines the sheath voltage above the wafer essentially independently of plasma generation. High bias powers generate large sheath voltages, and thus energetic ion bombardment of the wafer surface. In absence of an RF bias, the film quality and gap-filling performance are poor due to a jagged appearance of the sidewall film suggesting that it is very porous and heavy deposits forming above metal lines shadow the trench

bottoms from
deposition and eventually pinch-off the gap, leaving a void.

FIG. 5 shows an illustration of a deliberately layered gap-fill process of SiO.sub.2 in a gap 38 formed by Al lines 40 and wherein Si-rich layers 42 are produced by reducing the O.sub.2 flow by 50% for 2 seconds 5 times during the deposition. As is clearly evident, the process results in very low sidewall **deposition, bottom-up** progression of the fill, and roughly 45.degree. facets characteristic of sputtering. This tendency of the physical sputtering yield to maximize at 45.degree. off normal is beneficial for sub 0.5 .mu.m gap-filling because it prevents voids by preferentially removing the shoulders with minimal impact on the deposition rate on horizontal surfaces.

Electron cyclotron resonance plasma chemical vapor deposition (ECR-CVD) and transformer coupled plasma CVD (TCP-CVD) systems can be used to target the next generation intermetal **dielectric** (IMD) deposition market. TCP can generate a high density plasma (>1.times.10.sup.11 ions/cm.sup.3) and sustain it even at a very low pressure (<10 mTorr). The advantages of high density PECVD such as TCP-CVD include increased throughput, uniform ion and radical densities over large areas, and subsequent manufacturability of scaled-up reactors. When complemented with a separate RF biasing of the substrate electrode, TCP-CVD systems also allow independent control of ion bombardment energy and provide an additional degree of freedom to manipulate the plasma deposition process.

In the ECR-CVD or TCP systems, film growth occurs by an ion-activated reaction between oxygen species impinging onto the wafer from the

plasma source and
silane fragments adsorbed on the wafer. Using ECR/TCP-CVD,
sub-0.5 .mu.m, high
aspect ratio gaps can be filled with superb quality
SiO.sub.2 **dielectric** on 8"
diameter wafers. In essence, the ECR/TCP-CVD system
provides a manufacturable
intermetal **dielectric** CVD process that utilizes high
density plasmas.

US-PAT-NO: 6184158

DOCUMENT-IDENTIFIER: US 6184158 B1

TITLE: Inductively coupled plasma CVD

---------- KWIC ---------

A method of depositing a **dielectric** film on a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor. Gap filling between electrically conductive lines on a semiconductor substrate and depositing a cap layer are achieved. Films having significantly improved physical characteristics including reduced film stress are produced by heating the substrate holder on which the substrate is positioned in the process chamber.

The present invention relates to a method and apparatus for high-density plasma-enhanced chemical vapor deposition of semiconducting and **dielectric** films and more particularly to techniques for depositing such films into high aspect ratio gaps on semiconductor substrates such as silicon wafers having metal interconnection layers.

Plasma-enhanced chemical vapor deposition (PECVD) has been used for depositing intermetal **dielectric** layers at low temperatures in integrated circuit applications. A publication by M. Gross et al. entitled "Silicon dioxide trench filling process in a radio-frequency hollow cathode reactor", J. Vac. Sci. Technol. B 11(2), March/April 1993, describes a process for void-free silicon dioxide filling of trenches using a hollow cathode

reactor wherein
silane gas is fed through a top target which supports a low frequency (1 MHz),
low pressure (.about.0.2 Pa) oxygen and xenon discharge. In this process, high
ion bombardment and a low rate of gas phase reaction produce an ion induced
reaction with surface adsorbates, leading to directional oxide film growth
whereby trenches with one micron openings and aspect ratios up to 2.5:1 are
filled at rates over 400 .ANG./min.

A publication by P. Shufflebotham et al. entitled "Biased Electron Cyclotron
Resonance Chemical-Vapor Deposition of Silicon Dioxide Inter-Metal **Dielectric**
Thin Films," Materials Science Forum Vol. 140-142 (1993) describes a
low-temperature single step gap-filled process for use in inter-metal
dielectric (IMD) applications in wafers up to 200 mm in diameter wherein sub
-0.5 micron high aspect ratio gaps are filled with SiO.sub.2 utilizing an
O.sub.2 --Ar--SiH.sub.4 gas mixture in a biased electron cyclotron resonance
plasma-enhanced chemical-vapor deposition (ECR-CVD) system. That single step
process replaced sequential gap-filling and planarization steps wherein CVD
SiO.sub.2 was subjected to plasma etch-back steps, such technique being
unsuitable for gap widths below 0.5 microns and aspect ratios (gap
height:width) above 1.3:1.

Prior art apparatuses suffer from several serious disadvantages with respect to
IMD applications. ECR and helicon sources which rely on magnetic fields are
complex and expensive. Moreover, magnetic fields have been implicated to cause
damage to semiconductor devices on the wafer. ECR, helicon, and helical
resonator sources also generate plasmas remotely from the wafer, making it very

difficult to produce uniform and high quality films at the same time and also difficult to perform in-situ plasma cleans necessary to keep particulates under control without additional equipment. Furthermore, ECR, helicon and helical resonator, and domed inductively-coupled plasma systems require large, complex **dielectric** vacuum vessels. As a corollary scale-up is difficult and in-situ plasma cleaning is time consuming.

The present invention is directed to processes that employ an inductively coupled plasma-enhanced chemical vapor deposition (IC PECVD) high density plasma system. The system is compact, in-situ cleanable and produces high quality semiconductor and **dielectric** films.

In one aspect, the invention is directed to a method for filling gaps between electrically conductive lines on a semiconductor substrate comprising the steps of: providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor which can include a substantially planar induction coil; introducing a process gas which can include a noble gas into the process chamber wherein the amount of noble gas is sufficient to assist in gap filling; and growing a **dielectric** film on the substrate with **dielectric** film being deposited in gaps between electrically conductive lines on the substrate.

In another aspect, the invention is directed to a method for filling gaps between electrically conductive lines on a semiconductor substrate comprising the steps of: providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor which can include a substantially planar induction coil; filling gaps between

electrically
conductive lines on the substrate by: (i) introducing a first process gas which
can include a noble gas into the process chamber wherein the amount of noble
gas is sufficient to assist in gap filling; and (ii) growing a first **dielectric**
film in the gaps at a first deposition rate; and depositing a capping layer
comprising a second **dielectric** film onto the surface of said first **dielectric**
film by introducing a second process gas into the process chamber, said capping
layer being deposited at a second deposition rate that is higher than the first
deposition rate.

In a further aspect, the invention is directed to a method of depositing a
dielectric film on a substrate comprising the steps of: providing a substrate
in a process chamber of an inductively coupled plasma-enhanced chemical vapor
deposition reactor wherein the substrate is positioned on a substrate holder;
introducing a process gas which can include a noble gas into the process
chamber, wherein the amount of noble gas is sufficient to assist in depositing
the **dielectric** film; controlling the temperature on a surface of the substrate
holder; and energizing the process gas into a plasma state by inductively
coupling RF energy into the process chamber and growing a **dielectric** film on
the substrate.

In order to provide a vacuum in chamber 21, a turbo pump is connected to outlet
port 30 and a pressure control valve can be used to maintain the desired vacuum
pressure. Process gases can be supplied into the chamber by conduits 31, 32
which feed the reactant gases to gas distribution rings extending around the
underside of **dielectric** window 33 or the process gases can be supplied through

a **dielectric** showerhead window. An external ICP coil is located outside the chamber in the vicinity of the window is supplied with RF power by RF source 35 and associated circuitry 36 for impedance matching, etc. As is apparent, the external induction coil is substantially planar and generally comprises a single conductive element formed into a planar spiral or a series of concentric rings. The planar configuration allows the coil to be readily scaled-up by employing a longer conductive element to increase the coil diameter and therefore accommodate larger substrates or multiple coil arrangements could be used to generate a uniform plasma over a wide area. When a substrate is processed in the chamber, the RF source 35 supplies the coil 34 with RF current preferably at a range of about 100 kHz-27 MHz, and more preferably at 13.56 MHz and the RF source 26 supplies the lower electrode with RF current preferably at a range of about 100 kHz-27 MHz, and more preferably at 400 kHz, 4 MHz or 13.56 MHz. A large DC sheath voltage above the surface of a substrate can be provided by supplying RF power to the electrode.

RF bias is applied to the substrate to generate ion bombardment of the growing film during the gap filling step. The RF frequency can be anything above the value necessary to sustain a steady state sheath, which is a few hundred kHz. Substrate bias has numerous beneficial effects on film properties, and can also be used to simultaneously sputter the growing film in the gap-fill step. This allows narrow, high aspect ratio gaps to be rapidly filled with high quality **dielectric**. RF bias can be used during the cap layer deposition step.

The deposition of SiO.sub.2 into sub-0.5 micron high aspect ratio gaps by the

inventive process involves the simultaneous deposition and sputtering of SiO.sub.2. The resultant anisotropic **deposition** fills gaps from the **bottom-up** and the angular dependence of the sputtering yield also prevents the tops of the gaps from pinching off during **deposition**. An important feature of most high density plasma systems is that the bias power determines the sheath voltage above the wafer essentially independently of plasma generation. High bias powers generate large sheath voltages, and thus energetic ion bombardment of the wafer surface. In the absence of an RF bias, the film quality and gap-filling performance tend to be poor due to a jagged appearance of the sidewall film suggesting that it is very porous and heavy deposits forming above metal lines shadow the trench bottoms from deposition and eventually pinch-off the gap, leaving a void.

In ICP systems, SiO.sub.2 film growth occurs by an ion-activated reaction between oxygen species impinging onto the wafer from the plasma source and silane fragments adsorbed on the wafer. Using ICP-CVD, sub-0.5 .mu.m, high aspect ratio gaps can be filled with high quality SiO.sub.2 **dielectric** on 8 in. (20.32 cm) diameter wafers. In essence, the ICP-CVD system provides a manufacturable intermetal **dielectric** CVD process that utilizes high density plasmas.

It has been demonstrated that for high density PECVD, improved deposition rate and uniformity can be achieved by employing a gas distribution system which provides uniform, high flow rate delivery of reactant gases onto the substrate surface, to both increase the deposition rate and to minimize the chamber cleaning requirements. A suitable gas distribution system

is disclosed in
copending application Ser. No. 08/679,213, filed on Jul.
2s, 1996, entitled
"INDUSED ANI THERMALLY CONTROLLED PLASMA PROCESSING SYSTEM
AND METHOD FOR HIGH
DENSITY PLASMA CHEMICAL VAPOR DEPOSITION OF **DIELECTRIC**
FILMS," by Brian
McMillin et al., which application is incorporated herein.

The system further includes an antenna 150, such as the
planar multiturn coil
shown in FIG. 4, a non-planar multiturn coil, or an antenna
having another
shape, powered by a suitable RF source and suitable RF
impedance matching
circuitry inductively couples RF energy into the chamber to
provide a high
density plasma. The chamber may include a suitable vacuum
pumping apparatus
for maintaining the interior of the chamber at a desired
pressure. A
dielectric window, such as the planar **dielectric** window 155
of uniform
thickness shown in FIG. 4, or a non-planar **dielectric**
window, is provided
between the antenna 150 and the interior of the processing
chamber 140 and
forms the vacuum wall at the top of the processing chamber.

A primary gas ring 170 is provided below the **dielectric**
window 155. The gas
ring 170 may be mechanically attached to the chamber
housing above the
substrate. The gas ring 170 may be made of, for example,
aluminum or anodized
aluminum.

A secondary gas ring 160 may also be provided below the
dielectric window 155.
One or more gases such as Ar and O.sub.2 are delivered into
the chamber 140
through outlets in the secondary gas ring 160. Any
suitable gas ring may be
used as the secondary gas ring 160. The secondary gas ring
160 may be located
above the gas ring 170, separated by an optional spacer 165
formed of aluminum

or anodized aluminum, as shown in FIG. 4.

Alternatively, although not shown, the secondary gas ring 160 may be located below the gas ring 170, in between the gas ring 170 and the substrate 120, or the secondary gas ring 160 may be located below the substrate 120 and oriented to inject gas vertically from the chamber floor. Yet another alternative is that the Ar and O.sub.2 may be supplied through outlets connected to the chamber floor, with the spacer 165 separating the **dielectric** window 155 and the primary gas ring 170.

Another gas injection system that can be used employs a plurality of injectors as illustrated in FIG. 5. In this embodiment, the orifice 167A is oriented to introduce the gas along an axis of injection (designated "A") in a direction pointing away from the wafer 120A (and toward the **dielectric** window). The angle or axis of injection may be along the axis of the injector (designated "B") or, alternatively, at an angle of up to about 90 degrees or higher with respect to the axis of the injector. In this configuration, the axis of injection may range from about 5 to <90 degrees, preferably about 15 to 75 degrees, and most preferably, about 15 to 45 degrees from the plane of the substrate. This design retains the feature that the process gas is focused above the wafer which leads to high deposition rates and good uniformity, and further provides the advantage of reduced susceptibility to orifice clogging. The reduced potential of the orifice clogging thus allows more wafers to be processed before injector cleaning is required, which ultimately improves the wafer processing throughput.

The ICP PECVD system generates a high density, low pressure

plasma in a process
gas comprising components that form the semiconducting or
dielectric, and cap
films. The inventive process is applicable to depositing any suitable
semiconducting, **dielectric** and/or cap film including, for example, hydrogenated
amorphous silicon Si:H, silicon oxide SiO.sub.x, where x is 1.5 to 2.5, silicon
nitride, SiN, silicon oxyfluoride, SiO.sub.x F.sub.y where x is 1.5 to 2.5 and
y is 2 to 10, and mixtures thereof. It is understood that both stoichiometric
and non-stoichiometric compounds can be deposited and the values of x and y can
be controlled by regulating the process parameters such as, for example, the
choice of reactant gases and their relative flow rates. It is expected that
inorganic and organic polymers can also be deposited. A preferred **dielectric**
and cap film comprises SiO.sub.2. While the invention will be illustrated by
describing the deposition of SiO.sub.2, it is understood that the invention is
applicable to other films.

The components of the process gas will depend on the semiconducting and/or
dielectric film to be deposited. With respect to silicon-containing films the
process gas can comprise, for example, silane (SiH.sub.4), tetraethylorthosilicate (TEOS),
1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS),
disilane (Si.sub.2 H.sub.6) or other silicon-containing organometallic gases.
The process gas may include a noble gas preferably Ar, Kr, Xe, and mixtures
thereof to control plasma properties or sputtering rates particularly during
the gap filling step prior to depositing the cap layer. To incorporate
non-silicon components into the film, the process gas may include a reactant
gas such as, for example, H.sub.2, O.sub.2, N.sub.2, NH.sub.3, NF.sub.3,
N.sub.2 O, NO and mixtures thereof. Reactant gases may

also comprise boron
and/or phosphorous containing gases to produce
boro-phospho-silicate glass
(BPSG), boro-silicate glass (BSG), and phospho-silicate gas
(PSG) films.

The FTIR spectra, shown in FIG. 2, illustrate the relevance
of reactions I and
II. At low R, Si--OH and Si--HOH absorbance bands were
observed, but not for
Si--H. At high R, there was no detectable Si--OH, but both
Si--H and sub-oxide
(Si.sub.2 O.sub.3) Si--O bands were present. At
intermediate R, just on the
O.sub.2 -rich side of the critical range, there appears to
be minimal Si--OH
and Si--H incorporation. The intermediate R range is
optimum for achieving the
desired **dielectric** constant. The refractive index can also
be used as a gauge
for the preferred operating conditions since refractive
indices between 1.465
and 1.480 correspond to films having good **dielectric**
constants.

The SEMs shown in FIGS. 3A, 3B, 3C, and 3D show examples of
good and bad
gap-fill by ICP-CVD. FIG. 3A shows a partial fill
attempted with no bias
power. The porous film morphology and the "breadloaf"
appearance of the film
can be seen at the tip of the line. This eventually closes
over to leave a
void like that shown in FIG. 3B. These are also the
structures that are
preferentially sputtered away, since the sputtering yield
is a maximum at
45.degree.. FIG. 3B gives an example of unsuccessful fill
where bias power was
used, but the E/D was too low for the gap. Note that the
breadloaves closed
early in the process, leaving a large, deep gap. In FIG.
3C a tiny void formed
just before the gap filled can be seen next to an otherwise
identical gap that
filled successfully. In this case E/D was marginal. No
layering was done

deliberately by depositing a thin Si-rich layer periodically and decorating the sample with the appropriate stain to bring out the composition contrast. This clearly shows how the gap fills from the **bottom up**, with little sidewall **growth** compared to that on horizontal surfaces. The 45.degree. facets formed above the lines by sputtering are also clearly visible. FIG. 3D shows how a moderate E/D process (100 sccm Ar) completely filled an aggressive gap. This shows that ECR-CVD can fill aggressive structures.

growing a **dielectric** film by PECVD on the substrate, wherein the **dielectric** film fills substantially the gaps between electrically conductive lines on the substrate and wherein the gaps have a diameter of less than 0.5 .mu.m.

15. The method of claim 1, wherein the **dielectric** film comprises silicon oxide.

16. The method of claim 1 wherein the **dielectric** film comprises SiO.sub.2.

17. The method of claim 1, wherein the process gas includes a silicon and fluorine-containing reactants and the **dielectric** film comprises silicon oxyfluoride.

18. The method of claim 1, wherein the gas mixture includes a nitrogen-containing gas and the **dielectric** film comprises silicon oxynitride.

filling gaps between electrically conductive lines on the substrate by PECVD by introducing a first process gas comprising a noble gas and growing a first **dielectric** film in the gaps at a first deposition rate; and

after filling a major portion or substantially all of the

each gap with the first **dielectric** film, depositing by PECVD a capping layer comprising a second **dielectric** film onto the surface of said first **dielectric** film by introducing a second process gas comprising a noble gas into the process chamber, said layer being deposited at a second deposition rate that is higher than the first deposition rate wherein the gaps have a diameter of less than 0.5 .mu.m.

34. The method of claim 23, wherein the **dielectric** film comprises silicon oxide, the first and second process gases including a silicon reactant and an oxygen reactant, the second process gas containing higher amounts of the silicon and oxygen reactants than the first process gas.

35. The method of claim 23, wherein the **dielectric** film comprises silicon oxide, and the first process gas includes a higher amount of the noble gas than the second process gas.

39. A method of depositing a **dielectric** film substrate comprising the steps of:

energizing the process gas into a plasma state by inductively coupling RF energy into the process chamber and growing a **dielectric** film on the substrate by PECVD the **dielectric** film being deposited in gaps between electrically conductive lines on the substrate wherein the gaps have a diameter of less than 1.5 .mu.m and the **dielectric** film substantially fills the gaps.

41. The method of claim 37, wherein the **dielectric** film comprises silicon oxide.

42. The method of claim 37, wherein the **dielectric** film comprises SiO.sub.2.

43. The method of claim 37, wherein the process gas includes a silicon and fluorine-containing reactants and the **dielectric** film comprises silicon oxyfluoride.

44. The method of claim 29, wherein the gas mixture includes a nitrogen-containing gas and the **dielectric** film comprises silicon oxynitride.

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A method for depositing silicon dioxide between features has been achieved. The method may be applied intermetal dielectrics, interlevel **dielectric**, or shallow trench isolations. This method prevents **dielectric** voids, corner clipping, and plasma induced damage in very small feature applications. Features, such as conductive traces, are provided overlying a semiconductor substrate where the spaces between the features form gaps. A silicon dioxide liner layer is deposited overlying the features and lining the gaps, yet leaving the gaps open. The silicon dioxide liner layer depositing step is by high density plasma, chemical vapor deposition (HDP CVD) using a gas mixture comprising silane, oxygen, and argon. The argon gas pressure, chamber pressure, and the sputter rf energy are kept low. A silicon dioxide gap filling layer is deposited overlying the silicon dioxide liner layer to fill the gaps, and the integrated circuit device is completed. The silicon dioxide gap filling layer depositing step is by high density plasma, chemical vapor deposition (HDP CVD) using a gas mixture comprising silane, oxygen, and argon. The argon gas pressure and chamber pressure are kept low while the sputter rf energy is increased.

In HDP CVD, a traditional CVD process for depositing silicon dioxide is combined with a simultaneous sputtering process. As the silicon dioxide layer is deposited, it is also sputtered, or etched by the high-density plasma. By combining both a deposition and an etching action in the same process, a very dense and high quality silicon dioxide layer may be formed. In addition, since the etching component can be anisotropically controlled, that is, can etch in specific directions, the HDP CVD offers a significant advantage for deposition of silicon dioxide inside gaps or trenches. The etching component can reduce the **deposition** rate on vertical sidewalls such that the gap can be filled from the **bottom up** without the top of the gap closing or pinching off. This prevents the formation of voids or keyholes in the silicon dioxide layer.

As shown in the preferred embodiment, the present invention provides a very manufacturable process for depositing silicon dioxide between features in the manufacture of integrated circuit devices. The unique two step process makes possible the deposition of silicon dioxide **dielectric** layers between even very closely spaced features while preventing the adverse effects of void formation, corner clipping, and plasma induced damage.